

WHAT IS CLAIMED IS:

1. An offset control circuit for adjusting offset voltages contained in differential voltages that are input from a pair of differential voltage input terminals and outputting the
5 adjusted differential voltages from a pair of differential voltage output terminals, the offset control circuit comprising:

a voltage/current converting portion that includes the pair of differential voltage input terminals and a pair of differential current output terminals, that generates a pair of differential output currents corresponding to a potential difference between a pair of
10 differential input voltages input from the pair of differential voltage input terminals, and that outputs the pair of differential output currents from the pair of differential current output terminals;

an offset adjusting current-generating portion that includes a pair of offset adjusting current-output terminals connected to the pair of differential current output terminals of the
15 voltage/current converting portion, and at least two offset adjusting current-control terminals, that generates a pair of offset adjusting currents by being controlled by offset adjusting current control signals input from the offset adjusting current-control terminals, and that outputs the pair of offset adjusting currents from the pair of offset adjusting current-output terminals; and

20 a current/voltage converting portion that includes a pair of differential terminals connected to the pair of differential current output terminals of the voltage/current converting portion, the pair of offset adjusting current-output terminals of the offset adjusting current-generating portion and the pair of differential voltage output terminals, that feeds a current flowing between the two differential terminals constituting the pair of
25 differential terminals, that converts the current into a corresponding voltage, and that generates the converted voltage at the pair of differential voltage output terminals.

2. The offset control circuit according to claim 1,

wherein the voltage/current converting portion includes:

a pair of bias current sources connected to the pair of differential current output terminals;

5 a pair of first transistors whose first driving terminals are connected to the pair of differential current output terminals, respectively, and whose gates are both connected to a control terminal; and

a pair of second transistors whose first driving terminals are connected to second driving terminals of the pair of first transistors, respectively, whose gates are connected to
10 the pair of differential voltage input terminals, respectively, and whose second driving terminals are connected to a reference potential supplying point.

3. An offset control circuit for adjusting offset voltages contained in differential voltages that are input from a pair of differential voltage input terminals and outputting the
15 adjusted differential voltages from a pair of differential voltage output terminals, the offset control circuit comprising:

a voltage/current converting portion that includes

the pair of differential voltage input terminals,

a pair of differential current output terminals connected to the pair of differential
20 voltage output terminals,

a pair of bias current sources to which the pair of differential current output terminals are connected,

a pair of first transistors whose first driving terminals are connected to the pair of differential current output terminals and whose gates are connected to a pair of control
25 terminals and

a pair of second transistors whose first driving terminals are connected to second driving terminals of the pair of first transistors, whose gates are connected to the pair of

differential voltage input terminals, respectively, and whose second driving terminals are connected to a reference potential supplying point,

that generates a pair of differential output currents corresponding to a potential difference between a pair of differential input voltages input from the pair of differential voltage input terminals, and that outputs the differential output currents from the pair of differential current output terminals;

an offset adjusting current-generating portion that includes

a pair of offset adjusting current-output terminals connected to the first driving terminals of the pair of second transistors of the voltage/current converting portion, and

at least two offset adjusting current-control terminals,

that generates a pair of offset adjusting currents by being controlled by offset adjusting current-control signals input from the offset adjusting current-control terminals, and that outputs the pair of offset adjusting currents from the pair of offset adjusting current-output terminals; and

a current/voltage converting portion that includes

a pair of differential terminals connected to the pair of differential current output terminals of the voltage/current converting portion,

that feeds a current flowing between the two differential terminals constituting the pair of differential terminals, that converts the current into a corresponding voltage, and that generates the converted voltage at the pair of differential voltage output terminals.

4. The offset control circuit according to claim 1,

wherein the voltage/current converting portion includes:

a pair of bias current sources to which the pair of differential current output terminals are connected, respectively;

a pair of second transistors whose first driving terminals are connected to the pair of differential current output terminals, respectively, and whose gates are connected to the

pair of differential voltage input terminals, respectively;

a pair of first transistors whose first driving terminals are connected to second driving terminals of the pair of second transistors, respectively, whose gates are both connected to a control terminal and whose second driving terminals are connected to a reference potential supplying point; and

resistor means having a predetermined resistance and being connected between the second driving terminals of the pair of second transistors.

5. The offset control circuit according to claim 1,
wherein the voltage/current converting portion includes:

a pair of bias current sources to which the pair of differential current output terminals are connected, respectively; and

a pair of transistors whose first driving terminals are connected to the pair of differential current output terminals, respectively, whose gates are connected to the pair of differential voltage input terminals, respectively, and whose second driving terminals are connected to a reference potential supplying point.

6. The offset control circuit according to claim 1 or 3,
wherein the current/voltage converting portion is resistor means having a predetermined resistance and being connected between the pair of differential terminals.

7. The offset control circuit according to claim 1 or 3,
wherein the current/voltage converting portion includes:
a pair of third transistors whose first driving terminals are connected to the pair of differential terminals, respectively, and whose gates are both connected to an input/output current control terminal; and

a pair of fourth transistors whose first driving terminals are connected to second

driving terminals of the pair of third transistors, respectively, whose gates are connected to the pair of differential terminals, respectively, and whose second driving terminals are connected to a reference potential supplying point.

5 8. The offset control circuit according to claim 1 or 3,
 wherein the current/voltage converting portion is a fifth transistor that is connected
 between the pair of differential terminals and whose gate is connected to an input/output
 current control terminal.

10 9. The offset control circuit according to claim 1 or 3,
 wherein the offset adjusting current-generating portion includes:
 a current source; and
 a pair of sixth transistors whose second driving terminals are connected to the
 current source, whose gates are connected to two of the offset adjusting current-control
15 terminals, respectively, and whose first driving terminals are connected to the pair of offset
 adjusting current-output terminals, respectively.

10. The offset control circuit according to claim 1 or 3,
 wherein the offset adjusting current-generating portion includes n (n is a natural
20 number) sub-offset adjusting current-generating portions;
 wherein the sub-offset adjusting current-generating portions each include
 an offset adjusting current-control terminal to which a one-bit signal out of an n-bit
 register signal is input such that the one-bit signals do not overlap with each other;
 a current source; and
25 a pair of seventh transistors whose second driving terminals are connected to the
 current source, one of whose gates is connected to the offset adjusting current-control
 terminal, the other of whose gates is connected to the offset adjusting current-control

terminal via an inverter and whose first driving terminals are connected to the pair of offset adjusting current-output terminals, respectively; and

wherein a pair of sub-offset adjusting currents generated in each of the sub-offset adjusting current-generating portions are supplied to the pair of offset adjusting current-output terminals, respectively.

11. A signal processing device comprising:

the offset control circuit according to claim 1 or 3; and

a processing circuit that performs predetermined processing for a differential output

10 voltage whose offset voltage has been adjusted with the offset control circuit; wherein

the offset control circuit and the processing circuit are formed on a single chip.

12. The signal processing device according to claim 11,

wherein the signal processing device is a part of a DVD reproduction device;

15 wherein the offset control circuit adjusts an offset voltage contained in a signal read out from a DVD and outputs the adjusted signal as a differential output voltage; and

wherein the processing circuit includes:

a front-end having a filter that performs a filtering process on the differential output voltage whose offset voltage has been adjusted with the offset control circuit; and

20 a back-end that converts an output signal from the front-end into an image signal and an audio signal.